3D-SEM Measurements of Stacked-NW Transistors Using New eTilt Metrology Algorithm

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Development groups of advanced CMOS are confronted with 3D pattern characterization and monitoring challenges. Pattern height/depth and edge slope variations are known to impact the device electrical performance. 3D SEM metrology enables non-destructive measurements of pattern morphology. 3DAM, an European Project, was established to fund such development work.

In this work, we present the 3D SEM with eTilt imaging capabilities for height measurements based on the innovative metrology algorithm for characterization of the morphology of Stacked-NW Transistors (Stacked Nanowires). CD SEM height measurements of such pattern showed good correlation with the TEM measurements.
The traditional CD SEM Metrology algorithms are designed to measure Top View images. They use edge-based detection approach for the points corresponding to the features topography (Topo points) location definition. The height estimation is based on the edge width measurement at different tilts (5 and 12 degrees at standard setup). The height accuracy critically depends on the accuracy of the Topo points location estimation. When the SEM scans pattern, the edges yield more electrons than the surface and this phenomenon is the basis of CD SEM metrology. Tilted beam imaging is different than top view imaging, only the edge facing the primary beam is visible at the image. A new approach is required to detect the top and the bottom of the visible edge. The difference between the old and new algorithm is significant for 12 degrees tilt images, being the significant factor in the height accuracy. Using the new algorithm, we can now detect the edge points and measure the features heights much more accurately.

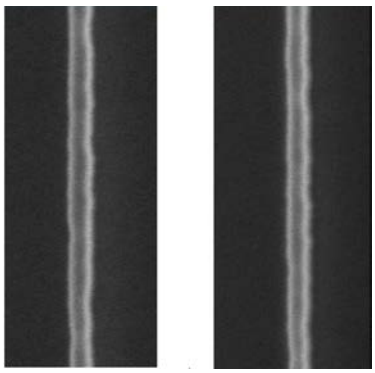
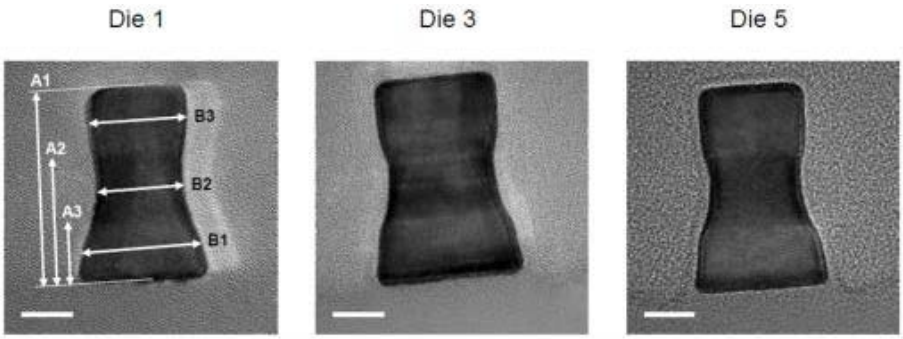


Figure 1. Stacked Nanowires with 5deg (on the left) and 12deg (on the right) tilt angle

In this work, we present a comparison of height measurements using the old and new algorithm. Comparing the results with TEM measurements, we could verify the accuracy of the algorithms and demonstrate the advantage of the new algorithm for height and edge slope measurements.

Experimental Setup: Stacked-NW device with the stack of Si/SiGe was generated with EPI and patterning (lithography and Etch) (Figure 1).
Pattern was measured with VeritySEM 4i+ using 5 and 12-degree electronic tilt (Figure I). Measurements were done using the old Line Analysis and new Tilt measurement algorithms. The final results are compared with TEM measurements.



+/- 0,5 nm	A1	A2	A3	B1	B2	B3
Die 1	38,7	25,0	12,3	23,5	17,0	19,2
Die 3	39,8	23,4	12,5	27,0	21,4	23,9
Die 5	40,6	26,7	13,2	24,7	18,3	20,8

Figure 2. TEM analysis

Results: We can observe the significant ~15nm difference on height measurement between the old and the new algorithms. Comparing to the TEM reference data, we reduced the offset to 1-2nm with the new algorithm providing basis for accurate 3D SEM Metrology.
Also, the new algorithm is able to follow the height variation. We can also observe that the new algorithm accurately follows roughness of the feature and it could be useful for other Tilt imaging based Process Control CD parameters measurements.

	Old algo	New algo	TEM
Die 1	21.64	37.34	38.7
Die 2	22.09	39.50	
Die 3	17.51	37.66	39.8
Die 4	18.77	38.38	
Die 5	23.81	38.94	40.6

Figure 3. Table comparison between CDSEM (for old and new algorithm) and TEM measurement